REMARKS

Claims 1-7, 9, 11-18, 20, and 23-25 are pending. Claims 1, 11, and 18 are amended. Claims 23-25 are new. Claim 21 is herein canceled without prejudice. Applicants submit that the amendments do not add new material to the current Application. No amendment made is related to the statutory requirements of patentability unless expressly stated herein. No amendment made is for the purpose of narrowing the scope of any claims, unless Applicants argue herein that such amendment is made to distinguish over a particular reference or combination of references.

Applicant notes that in the pre-appeal brief conference request it mistakenly referred to only the 35 U.S.C. § 103 rejection and not the 35 U.S.C. § 102 rejection. However, the arguments presented in the request addressed both rejections. Applicants wish to point out for the record that currently there are two rejections: one under 35 U.S.C. § 102 and another under 35 U.S.C. § 103.

Claims 1, 2, 9, 11, 12, 17, 18, 20, and 21 are patentable under 35 U.S.C. 102(b) over Kono (U.S. 5,972,756).

Claims 1, 2, and 9

Applicant submits that Kono fails to teach all features of claim 1 and its dependencies, especially claims 2 and 9. For example, Kono fails to teach or suggest, "a passivation layer formed overlying at least a portion of the substrate, wherein the passivation layer is not under a dielectric layer."

First, Applicants submit that Kono's interlayer 124 is not a passivation layer. The USPTO must interpret a claim term using its plain meaning unless the interpretation is inconsistent with the specification. MPEP § 2111.01(I). The plain meaning of a term is the ordinary and customary meaning that a skilled artisan at the time of the invention would give to the term. MPEP § 2111.01(III). "The ordinary and customary meaning of

a term may be evidenced by a variety of sources, including "the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art." *Phillips v. AWH Corp.*, 415 F.3d at 1314, 75 USPQ2d at 1327.

Applicant submits that the Examiner is not applying the plain meaning of the phrase "passivation layer." More specifically, the Examiner is not interpreting the phrase "passivation layer" to mean the ordinary and customary meaning that a skilled artisan at the time of the invention would give to the term. The Examiner contends that the term "passivation layer" applies to any layer that overlies an ILD (interlayer dielectric) layer. The Examiner is ignoring the plain meaning of the term "passivation layer." *Phillips* outlines what materials should be referenced to determine the plain meaning. When considering the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of "passivation layer" is not any layer that overlies an ILD (interlayer dielectric) layer, as the Examiner contends. Instead, it is the last dielectric material or layer (which can be a multiple layer dielectric layer). Applicant's specification supports this by stating that a passivation layer protects the underlying layers from physical handling of the semiconductor device and the environment. (See page 6, lines 18-22 of Applicant's specification). Furthermore, a book used to teach courses at Yale University and the University of Texas-Austin states that a passivation layer is a layer that is formed in "One of the final stages in the integrated circuit fabrication process" and involves "the entire surface of the wafer [being] coated with a layer of silicon dioxide or silicon nitride." (Maxfield, Clive, *Behop to the Boolean Boogie: An Unconventional Guide to Electronics,* Electronics Glossary of "Overglassing" which the definition of "Passivation layer" points to). A copy of the glossary with an excerpts from the book is attached for the Examiner's convenience. Kono's interlayer dielectric 124 does not protect the underlying layers from physical handling of the semiconductor device and the environment. Furthermore, it is not formed during one of the final stages of the integrated circuit fabrication process. In contrast, Kono forms many additional

processes, such as forming additional dielectric layers 143 and 150 over the interlayer 124.

As discussed above, one reason Kono's interlayer 124 is not a passivation layer is that it is under a dielectric layer. While Applicant believes claim 1 and its dependencies were allowable without the amendment to claim 1, such amendments were added to hasten the final decision of this prolonged prosecution, which has already taken over six years. Hence, Applicant has amended claim 1 to state that the passivation layer is not under a dielectric layer. Kono's interlayer 124 is under dielectric layers 143 and 150 and hence, Kono's interlayer 124 cannot be the passivation layer of Applicant's claims. Thus, Kono fails to teach, "a fuse, formed overlying and in contact with the passivation layer." Kono's fuse 130 is under Kono's passivation layer 150.

For at least these reasons, claim 1 and its dependencies, especially claims 2 and 9, are patentable over Kono under 35 U.S.C. 102(b).

Claims 11, 12, and 17

Applicant submits that Kono fails to teach all features of claim 11 and its dependencies, especially claims 12 and 17. For example, Kono fails to teach, "a passivation layer formed overlying at least a portion of the substrate, wherein the fuse is formed overlying the passivation layer; and a packaging material formed in contact with an entire length of the fuse," as sated in claim 11. (While Applicant believes claim 11 and its dependencies were allowable without the amendments to claim 11, such amendments were added to hasten prosecution.)

First, Applicants submit that Kono fails to teach "a passivation layer formed overlying at least a portion of the substrate, wherein the fuse is formed overlying the passivation layer;" because, as discussed above and not repeated for brevity, Kono's interlayer 124 is not a passivation layer. Instead, Kono's passivation layer is dielectric layer 150, and Kono's fuse 130 is not overlying the passivation layer 150, which is a feature of claims 11 and its dependencies.

Second, Kono fails to teach, "a packaging material formed in contact with an entire length of the fuse." If Kono was to put a resin over its package the resin would not be in contact with an entire length of the fuse because the length of the fuse would also be in contact with the dielectric layer 140. (See Kono's FIG. 1.)

For at least these reasons, claim 11 and its dependencies, especially claims 12 and 17, are patentable over Kono under 35 U.S.C. 102(b).

Claims 18, 20 and 21

Applicant submits that Kono fails to teach all featured of claim 18 and its dependencies, especially claims 20 and 21. For example, Kono fails to teach, "(forming) a passivation layer overlying at least a portion of the substrate, wherein the passivation layer is not formed under a dielectric layer," as discussed in regards to claim 1 and its dependencies. Therefore claim 18 and its dependencies are patentable over Kono under 35 U.S.C. 102(b) for at least the same reasons as claim 1 and its dependencies.

In addition, the Applicant believes claim 18 and its dependencies were allowable without the amendment to claim 18. However, the amendment to claim 18 was made solely to hasten prosecution.

Claims 3-7 and 13-16 are patentable under 35 U.S.C. 103(a) over Kono (U.S. 5,972,756) in view of Weber (6,218,279).

Applicant respectfully submits claims 3-7 and 13-16 are patentable under 35 U.S. 103(a) over Kono and Weber because the references fail to teach or suggest all features of the claims, especially the features of independent claims 1 and 11, from which claims 3-7 and 13-16 depend.

As discussed above, with respect to claim 1 and its dependencies, Kono fails to teach, "a passivation layer formed overlying at least a portion of the substrate, wherein the passivation layer is not under a dielectric layer; [and] a fuse, formed overlying and in contact with the passivation layer," as stated in claim 1. Kono and Weber, alone or together, fail to suggest these features because the combination teaches forming a fuse under a passivation layer.

As discussed above, with respect to claim 11 and its dependencies, Kono fails to teach, a passivation layer formed overlying at least a portion of the substrate, wherein the fuse is formed overlying the passivation layer; and a packaging material formed in contact with an entire length of the fuse," as stated in claim 11. Kono and Weber, alone or together, fail to suggest these features because the combination teaches forming a fuse under a passivation layer and the combination also teaches a fuse in contact with only a portion of the length of the fuse.

For at least these reasons, claims 3-7 and 13-16 are patentable under 35 U.S. 103(a) over Kono and Weber.

New Claims

The new claims are patentable for at least the same reasons the claims from which they depend are patentable. In addition, the new claims are patentable for additional reasons. For example, Kono and Weber fail to teach or suggest, "wherein the packaging material is in contact with an entire surface of the fuse," as stated in claims 24, and "wherein forming the fuse further comprises forming the fuse in contact with an entire surface of the fuse," as stated in claim 25.

The Office Action contains numerous statements characterizing the claims, the specification, and the prior art. Regardless of whether such statements are addressed by Applicants, Applicants refuse to subscribe to any of these statements, unless expressly indicated by Applicants.

Applicants earnestly solicit allowance of all pending claims.

Respectfully submitted,

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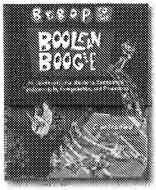

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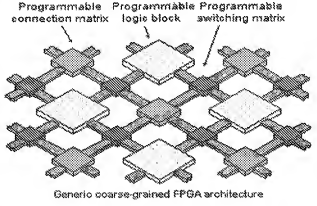

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Padcap

A special flavor of circuit board used for high-reliability military applications. Distinguished by the fact that the outer surfaces of the board have pads but no tracks. Signal layers are only created on the inner planes, and tracks are connected to the surface pads by vias.

Pad

An area of metalization on a substrate used for probing or to connect to a via, plated through-hole, or an external interconnect.

Pad Grid Array (PGA)

A packaging technology in which a device's external connections are arranged as an array of conducting pads on the base of the package.

Pad Stack

Refers to any pads, anti-pads, and thermal relief pads associated with a via or a plated through-hole as it passes through the layers forming the substrate.

Parallel-In Serial-Out (PISO)

Refers to a shift register in which the data is loaded in parallel and read out serially.

Parasitic Effects

The effects caused by undesired resistance, capacitance, or inductance inherent in the material or topology of a track or component.

Passivation Layer (see *Overglassing*)

Passive Trimming

A process in which a laser beam is used to trim components such as thick-film and thin-film resistors on an otherwise unpopulated and unpowered hybrid or multichip module substrate. Probes are placed at each end of a component to monitor its value while the

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Octal

Base-8 numbering system. Each octal digit can be directly mapped onto three binary digits, or bits.

Ohm

Unit of resistance. The Greek letter omega, Ω, is often used to represent ohms; for example, 1MΩ indicates one million ohms.

One-Hot Encoding

A form of state assignment for state machines in which each state is represented by an individual state variable.

One-Time Programmable

A device such as a PAL, PLA, or PROM that can only be programmed a single time and whose contents cannot be subsequently erased.

Operating System

The collective name for the set of master programs that control the core operation and the base-level user-interface of a computer.

Optical Interconnect

The generic name for interconnection strategies based on opto-electronic systems, including fiber-optics, free-space, guided-wave, and holographic techniques.

Optical Lithography

A process in which radiation at optical wavelengths (usually in the ultraviolet range) is passed through a mask, and the resulting patterns are projected onto a layer of resist coating the substrate material.

Optical Mask

A sheet of material carrying patterns that are either transparent or opaque to the

wavelengths used in an optical-lithographic process. Such a mask can carry hundreds of thousands of fine lines and geometric shapes.

Opto-Electronic

Refers to a system which combines optical and electronic components.

Organic Resist

A material which is used to coat a substrate and is then selectively cured to form an impervious layer. These materials are called organic because they are based on carbon compounds as are living creatures.

Organic Solvent

A solvent for organic materials such as those used to form organic resists.

Organic Substrate

Substrate materials such as FR4, in which woven glass fibers are bonded together with an epoxy. These materials are called organic because epoxies are based on carbon compounds as are living creatures.

Overglassing

One of the final stages in the integrated circuit fabrication process in which the entire surface of the wafer is coated with a layer of silicon dioxide or silicon nitride. This layer may also be referred to as the barrier layer or the passivation layer. An additional lithographic step is required to pattern holes in this layer to allow connections to be made to the pads.

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